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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,497	12/30/2003	Joseph Farley	TI-36217	8748

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EXAMINER	
TRAN, MAI HUONG C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 04/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

A·A

Office Action Summary	Application No.	Applicant(s)	
	10/748,497	FARLEY ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The specification is objected to for the following reasons.

Typographical error has been found on page 6, line 24, "...overlies **an a** VTN...". Correction is required.

'**VTN** p-diffusion' should be spelled out.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 6 and 8 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,762,453 to Simacek et al.

Regarding to claim 1, Simacek discloses an electronically erasable read only memory comprising a capacitor 38 comprising a diffusion layer 44 of a first conductivity

type formed in a well 14 of a second conductivity type; an insulating layer 48 overlying the diffusion layer 44; and a floating gate 46 overlying the diffusion layer 44; and a MOS transistor 18 comprising first and second active regions 20, 22 formed in the well 14, adjacent to an extended portion of the floating gate 26/46 (col. 4, lines 26-52, and fig. 2).

Regarding to claim 3, Simacek discloses the electronically erasable read only memory wherein the first conductivity type is an n type and the second conductivity type is a p type (P-well 14, N-type diffusion 44: col. 4, lines 33-52).

Regarding to claim 6, Simacek discloses a method of forming an electronically erasable read only memory comprising the steps of forming a diffusion layer 44 of a first conductivity type formed in a well 14 of a second conductivity type; forming an insulating layer 48 overlying the diffusion layer 44; and forming a floating gate 46 overlying the diffusion layer 44; and forming first and second active regions 20, 22 formed in the well 14, adjacent to an extended portion of the floating gate 26/46 (col. 4, lines 26-52, and fig. 2).

Regarding to claim 8, Simacek discloses the method wherein the step of forming a diffusion layer comprises the step of forming a diffusion layer of an n conductivity type in a well of a p conductivity type (col. 4, lines 26-52, and fig. 2).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 7 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,762,453 to Simacek et al. in view of the remark.

Regarding to claims 2 and 7, Simacek discloses the claimed invention except for the electronically erasable read only memory wherein the first conductivity type is a p type and the second conductivity type is an n type. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electronically erasable read only memory wherein the first conductivity type is a p type and the second conductivity type is an n type, since it has been held that a mere reversal of the essential working parts of a device involves only routine skill in the art. In re Einstein, 8 USPQ 167.

Claims 4-5 and 9-10 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,762,453 to Simacek et al. in view of Sugaya Fumitaka (US 6,232,182).

Regarding to claims 4 and 9, Simacek discloses the claimed invention except for the electronically erasable read only memory further comprising a second diffusion layer beneath one of the first and second active regions. However, Sugaya teaches the electronically erasable read only memory further comprising a second diffusion layer 8 beneath one of the first and second active regions (col. 4, lines 50-67, col. 5, lines 1-15, and fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electronically erasable read only memory further comprising a second diffusion layer beneath one of the first and second active regions, as taught by Sugaya in order to provide a non-volatile semiconductor memory device, such as an EEPROM and flash memory, which is capable of rewriting at high speed and preventing the reduction of the breakdown voltage of the PN junction between the drain and the substrate, and/or the hot carrier deterioration, thereby increasing the reliability, and to a method of manufacturing such a memory device (col. 2, lines 45-52).

Regarding to claims 5 and 10, Simacek discloses the claimed invention except for the electronically erasable read only memory wherein the first active region comprises a

source, the second active region comprises a drain, and the extended portion the floating gate comprises a gate of a MOS transistor, and the second diffusion layer is formed beneath the second active region. However, Sugaya teaches the electronically erasable read only memory wherein the first active region comprises a source, the second active region comprises a drain, and the extended portion the floating gate comprises a gate of a MOS transistor, and the second diffusion layer is formed beneath the second active region (col. 4, lines 50-67, col. 5, lines 1-15, and fig. 1).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electronically erasable read only memory wherein the first active region comprises a source, the second active region comprises a drain, and the extended portion the floating gate comprises a gate of a MOS transistor, and the second diffusion layer is formed beneath the second active region, as taught by Sugaya in order to provide a non-volatile semiconductor memory device, such as an EEPROM and flash memory, which is capable of rewriting at high speed and preventing the reduction of the breakdown voltage of the PN junction between the drain and the substrate, and/or the hot carrier deterioration, thereby increasing the reliability, and to a method of manufacturing such a memory device (col. 2, lines 45-52).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran